Distributed Architecture for Robust and Optimal Control of DC Microgrids

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Abstract—This article presents a distributed, robust and optimal control architecture for a network of multiple DC-DC converters. The network of converters considered form a DC microgrid in order to regulate a desired DC bus voltage and meet prescribed time-varying power sharing criteria among different energy sources. Such coordinated microgrids provide an important framework for leveraging the benefits of distributed power generation and consumption. The proposed control design seamlessly accommodates communication architectures that range from centralized to decentralized scenarios with graceful degradation of performance with lessened communication ability. Moreover, methods developed are applicable to the case where the desired proportion in which the sources provide power varies with time. A distinguishing feature of the control design approach is that it regards the net load current as a *disturbance* signal, lending itself to tractable analysis with tools from robust and optimal control theory. A quantifiable analysis of the closed-loop stability and performance of the network of converters is performed; the analysis simplifies to studying closed-loop performance of an equivalent single-converter system. The control approach is demonstrated through simulations and experiments.

Index Terms—Microgrid, Converters, Power Sharing, Robust Control, Distributed Control.

I. INTRODUCTION

INCREASING use of renewable generation and distributed energy resources (DERs), such as residential solar, and electric vehicles coupled with customers' changing energy usage patterns are leading to greater uncertainty and variability in the electric grid. New flexible architectures are required that can accommodate the increase in renewable generation and DERs, while providing the quality of service, resiliency, and reliability that customers expect.

Coordinated microgrids provide an important framework for leveraging benefits of distributed power generation and consumption. Microgrids also help mitigate challenges arising from DERs penetration into the grid

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by enabling management of demand response and generation [2], [3]. Fig. 1 shows a schematic view of a
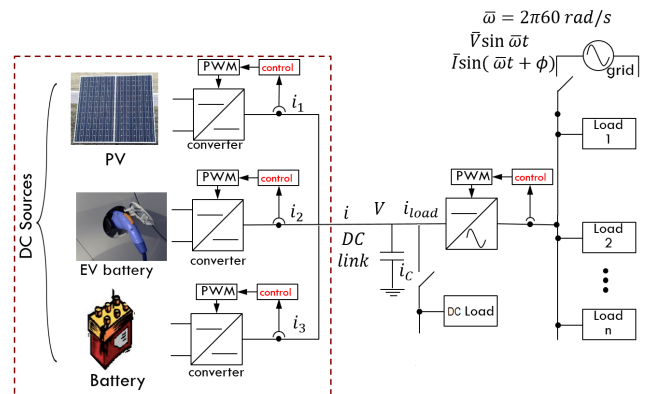

Fig. 1: A schematic of a microgrid. A network of multiple DC sources are arranged in parallel through an array of DC-DC converters to regulate voltage and provide power at the DC-link. The DC-link either interfaces with DC loads directly, or to a DC/AC inverter to satisfy the power demands of AC loads.

microgrid system with multiple DC sources in parallel. The power aggregated at the DC-link can directly feed DC loads, and can be used by a DC-AC inverter to interface with AC loads and the utility grid. The voltage and power at the DC-link is manipulated by suitably controlling duty-cycle of the switches of DC-DC converters at each power source. The primary objectives of controller are to regulate the voltage at the DC-link, while ascertaining that the various power generation sources are utilized in the specified priority order and proportion to meet the load demand.

The main challenges in the control of microgrids arise from uncertainties in renewable power sources such as, solar and wind due to intermittent power generation, uncertainties in load demands and schedules, and in distributed topology of power sources that are spatially scattered due to location and size constraints. In view of these challenges, a robust and distributed control technology is needed for reliable operation of smart microgrids. In the multiple-input multiple-output setting necessitated by the need to control multiple generation sources, it is difficult to address robustness and performance criteria in the conventional PID-based control synthesis framework. Recently robust and optimal

control methodologies have received attention. In [4], a linear-matrix-inequality (LMI) based robust control design is presented for boost converters which demonstrates significant improvements in voltage regulation over PID based control designs. In [5]–[7], robust $\mathcal{H}_\infty$-control framework is employed in the context of inverter systems. While the issue of current sharing is extensively studied (see [8] and [9]), most prior methods reported assume a single power source. Our preliminary work [10] uses tools from robust control theory [11], [12] to partially address control objectives pertaining to managing multiple generation sources. However, a major drawback of the design suggested in [10] is that it fails to provide analyzable guarantees to time-varying power sharing requirements, and is thus suited for cases where power sharing is required in a fixed prespecified proportion. Although, there is significant literature on control and power management techniques for AC microgrids [13], [14], recent works [15], [16] have emphasized the importance of DC microgrids due to their islanding capabilities in presence of voltage fluctuations and capability to facilitate integration of DERs. In this article, we present a distributed robust control architecture for a network of parallel DC-DC converters that simultaneously addresses multiple objectives of regulating the DC link voltage and ascertaining that the specification on the prioritization and proportion of power generation are met robustly in the presence of modeling, power generation, and load demand uncertainty.

The main contributions of this article are (a) *robust regulation and sharing performance*: Appropriate maps of the duty cycle are identified that facilitate a common framework for analyzing and synthesizing controllers for different types of converters while rendering models that are linear. Modern robust control tools are employed to to address multiple objectives that include regulation of the DC-link voltage to a desired set-point reference, and a prescribed sharing of power among different DERs. The sharing requirements can be time-varying and are often dictated by the availability and relative costs of different power sources. Our architecture allows sharing specifications that include priorities on the order in which different sources and loads are utilized. For example, a priority specification of the form, PV $\prec$ Battery $\prec$ EV, is natural which codifies the following objective: irrespective of the changing power generation of the PV, the state of charge of the battery and the EV, the EV will source power only if the battery and the PV cannot meet the power demand, while the battery sources power only if the PV is not able to meet the load demand. Apart from meeting performance guarantees including prioritization, our control design also addresses the challenges of interfacing AC loads, including the 120 Hz ripple that has to be provided by the DC sources. It provides a means for achieving a trade off between the 120 Hz ripple on the total current provided by the power sources and the ripple on the DC-link voltage.

The networked system resulting from our architecture is robust to uncertainties in load demands and schedules, communication topologies, system parameters, and noise in measurement signals. (b) *modular and structured architecture*: The control architecture presented in this work is modular and facilitates plug and play operation. Here, a new converter module can be added or removed from the network, without any need to redesign controllers and without compromising the voltage regulation performance of the network. Furthermore, adding a module, which is agnostic to sharing ratios of other modules, to the networked system does not affect the overall performance of the networked system. The intra-module and inter-module control is structured in such a way that it allows easy multi-converter network analysis and synthesis. In the framework developed, the network of parallel converters can be analyzed, and the corresponding control systems synthesized, in terms of an *equivalent* single-converter system. (c) *robustness to communication uncertainties*: The synthesis procedure results in a single controller which functions for the entire range of communication capabilities; from decentralized to centralized. Here, it guarantees precise regulation of the DC-link voltage and power sharing specifications when communication allows for a centralized operation, and meets gracefully degraded specifications with lessened communication capabilities among converters.

II. PRELIMINARIES: FACILITATING LINEAR MODELS OF DC-DC CONVERTERS

Fig. 2a shows a schematic of a boost converter with output voltage V and input voltage V_g. If $d(t)$ represents the duty-cycle (or the proportion of *ON* duration) for the semiconductor switch at time t, then the averaged dynamic model of a boost converter is described by:

$$L\frac{di_L(t)}{dt} = -(1-d(t))V(t) + V_g,$$
$$C\frac{dV(t)}{dt} = (1-d(t))i_L(t) - i_{\text{load}}(t), \qquad (1)$$

where, $i_L(t)$ is the averaged inductor current, and L and C denote the converter inductance and capacitance, respectively [17], [18]. By defining $d'(t) \triangleq 1 - d(t)$ as the complementary duty-cycle and $D' \triangleq (V_g/V_{\text{ref}})$, where $V_{\text{ref}} > V_g$ is the desired output voltage, (1) can be rewritten as:

$$L\dot{i}_L(t) = \tilde{u}, \qquad C\dot{V}(t) = \underbrace{(D' + \hat{d}(t))}_{\approx \alpha} i_L(t) - i_{\text{load}}(t), \quad (2)$$

where $\tilde{u}(t) := V_g - d'(t)V(t)$. In this model, the constant $\alpha = D'$ approximates the term $D' + \hat{d}(t)$, since $\hat{d}(t) = d'(t) - D'$ is typically small. Note that the equivalent duty cycle $d(t)$ can be obtained from $\tilde{u}$ via $d(t) = 1 - \dfrac{V_g - \tilde{u}(t)}{V(t)}$. In (2) load current i_{load} appears as a *disturbance* signal, and thus an appropriate controller can be synthesized for rejecting this disturbance.

The averaged dynamical equations for other converter topologies (see Figs. 2b and 2c) can be derived in a similar manner, and they result in dynamic models that are structurally identical to the boost converter model
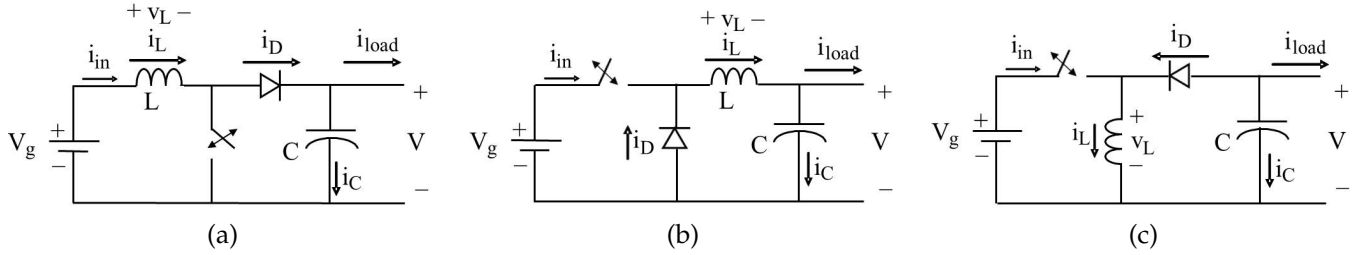
Fig. 2: Circuit representing (a) Boost converter, (b)Buck converter, and (c) Buck-Boost converter. Voltage V at the output is regulated by repeatedly turning ON/OFF the switch between input and output. Note that i_{load} includes both the nominal load current, as well as ripple current. The converters are assumed to operate in continuous-conduction-mode (CCM).

(2). Buck converter results in the same dynamic model as (2) with $\tilde{u} = -V(t) + d(t)V_g$ and $\alpha = 1$. Similarly, the buck-boost converter is modeled by (2) with $\tilde{u} = V(t) + d(t)(V_g - V(t))$ and $\alpha = -D'$.

Remark: Note that the way the input variables $\tilde{u}$ are chosen in these models is critical which results in linear dynamic model (2) even though the maps from original control input $d(t)$ to inductor current and voltage are non-linear. This structure enables linear control design, where $\tilde{u}(t)$ is synthesized, and the corresponding duty-cycle be implemented is determined using the invertible map between $\tilde{u}$ and $d(t)$. Since the averaged models for the boost, buck, and buck-boost converters are structurally identical, one can easily derive the control design of one from the other. For brevity and as a result of this equivalence, we present a control design method for boost-type converters.

III. CONTROL OBJECTIVES AND DESIGN

The proposed work simultaneously addresses the following primary objectives (in the context of Figs. 1 and 2) : (a) Effective regulation of the DC-link voltage V to a pre-specified setpoint value V_{ref} in presence of time-varying loads (manifested through i_{load}), uncertainties in input voltage V_g, and parametric uncertainties in L and C values, (b) Time-varying current (power) sharing among multiple sources that ensures that current (power) outputs i_k from the kth converter tracks a time-varying signal i_{ref_k}, and (c) Managing 120 Hz ripple current trade-off between the total current, $i = \sum i_k$ sourced by DC sources and the DC-link capacitor current i_C. Note that in this network, each controller interfaced with a DC-DC converter has access to its own measurement of the DC-link voltage V and its inductor current. Furthermore, each controller is provided with a reference voltage command V_{ref}, common nominal reference current i_{ref}, and power-sharing proportion γ_k (see Fig. 4). Also the uncertain exogenous input at k^{th} converter is $i_{\text{load}} - \sum_{j \neq k} i_j$, which is equal to $(1 - \gamma_k)i_{\text{load}}$, when all the controllers are satisfying the power sharing requirements. In such a case, the knowledge of $i_{\text{load}}(t)$ is sufficient for voltage regulation and power sharing objectives. Therefore in the centralized setting, it is assumed that a controller can additionally measure or estimate the net load current i_{load}, and set $i_{\text{ref}} = i_{\text{load}}$. In the decentralized case i_{load}

is not known at each controller (i_{ref} is set at a nominal value). We first describe a control scheme for a single converter which forms a basis for the analysis and design of distributed control architecture for a system network of multiple converters in parallel described in Section III-B.

A. Control Design for Single Converter

Fig. 3 depicts a block diagram representation of the the proposed inner-outer control design. Note that a cascade inner-current outer-voltage control architecture is preferred over a traditional single measurement controller for voltage tracking and load disturbance rejection, primarily due to fast current dynamics over slow voltage dynamics [19], [20]. In fact, it is shown in [21] that the cascaded inner-current outer-voltage structure is an optimal strategy in terms of voltage regulation and robustness, when both bus voltage V and inductor current i_L are measured. The inner controller is designed to achieve fast rejection to disturbance in current arising due to variations in the output load, while the primary outer controller regulates the output voltage by generating the required set-point for the inner loop. Thus the inner current controller influences the outer voltage loop by affecting the primary process variable (voltage signal) in a predictable and repeatable way. Here K_c represents the inner-loop controller which addresses the ripple-current management objective, while $[K_v, K_r]$ constitute the outer-loop controllers to address the DC-link voltage regulation and power sharing objectives. The requirements on current sharing are imposed through the exogenous input i_{ref} (explained in Sec. III-B). i_{ref} is set to the measured (or communicated) value of load current i_{load} when available, while in the absence of i_{load} measurement, i_{ref} is set to pre-specified nominal value.

1) Design of inner-loop controller: The primary objectives for designing the inner-loop controller K_c is to achieve the desired trade-off between the 120 Hz ripple on the capacitor current i_C (or equivalently on the output voltage V) and the inductor current i_L (see Fig. 2a), and ensure robust tracking of the command $\hat{u}$ (in Fig. 3) by the inductor current i_L. The signal $\hat{u}$ is the reference command generated by the outer-voltage controllers for the inner-controller that regulates i_L. Here, K_c is designed
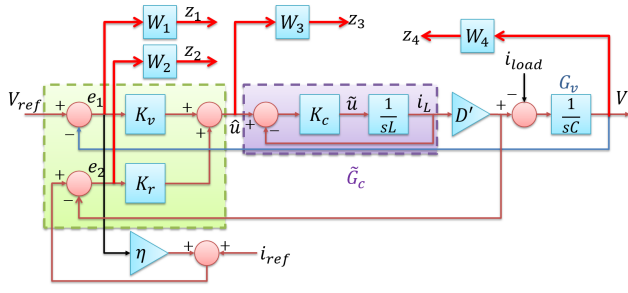
Fig. 3: Block diagram representation of the inner-outer control design. Exogenous signal V_{ref} represents the desired output voltage. The quantities V, i_{load} and i_L represent the output voltage, load current and inductor current, respectively. The *regulated variables* z_1, z_2, z_3 and z_4 correspond to weighted - (a) tracking error in DC-link voltage, (b) mismatch between i_{ref} and i_{load}, (c) control effort $\hat{u}$, and (d) output voltage tracking, respectively. $G_v(s) \triangleq \frac{1}{sC}$ represents the plant transfer function from DC-link capacitor current to output voltage V.

such that the transfer function $\tilde{G}_c$ (from $\hat{u}$ to i_L) in Fig. 3 is given by:

$$\tilde{G}_c(s) = \left(\frac{\tilde{\omega}}{s + \tilde{\omega}} \right) \left(\frac{s^2 + 2\zeta_1 \omega_0 s + \omega_0^2}{s^2 + 2\zeta_2 \omega_0 s + \omega_0^2} \right), \qquad (3)$$

where $\omega_0 = 240\pi$ rad/s and $\tilde{\omega}, \zeta_1, \zeta_2$ are design parameters. Parameter $\tilde{\omega} > \omega_0$ is chosen to implement a low-pass filter that attenuates undesirable frequency content in i_L beyond $\tilde{\omega}$ resulting from noisy measurements and switching effects. $\tilde{G}_c(s)$ also incorporates a notch at $\omega_0 = 120$ Hz, where the "size" of the notch is determined by the ratio ζ_1/ζ_2. Lower values of this ratio correspond to a larger notch magnitude, which in turn implies smaller 120 Hz component in i_L. Since $i_C = C\dot{V} = D'i_L - i_{\text{load}}$, the 120 Hz ripple in the load current is reflected as a larger ripple in V, when the proportion in i_L is pushed lower. Thus the ratio ζ_1/ζ_2 regulates the trade-off between 120 Hz ripple on inductor current i_L and DC-link voltage V. The stabilizing second-order controller K_c that yields the inner-closed loop plant $\tilde{G}_c$ is given by:

$$K_c(s) = L\tilde{\omega} \frac{(s^2 + 2\zeta_1 \omega_0 s + \omega_0^2)}{(s^2 + 2\zeta_2 \omega_0 s + \omega_0^2 + 2(\zeta_2 - \zeta_1)\omega_0 \tilde{\omega})}. \qquad (4)$$

The readers are encouraged to refer to Sec. III in [10] for further details on the inner-loop control design.

2) Design of outer-loop controller: For a specified inner closed-loop plant $\tilde{G}_c$ in (3), we now present a systematic design for the outer controllers, $[K_v \ K_r]$, shown in Fig. 3. The fundamental performance limitations of the proposed closed-loop design with inner closed-loop plant $\tilde{G}_c \triangleq \frac{K_c}{sL + K_c}$ and outer controllers $[K_v \ K_r]$ is analyzed below by investigating the closed-loop dynamical equation from reference voltage V_{ref}, reference current i_{ref} and load-current i_{load} to DC-link voltage V. Furthermore, the closed-loop dynamics provides useful insights into the control methodology and explains how the same architecture with identical controllers work for both matched ($i_{\text{ref}} = i_{\text{load}}$) and unmatched ($i_{\text{ref}} \neq i_{\text{load}}$) conditions. Note that from Fig. 3, the DC-link voltage V is given by,

$$V = G_v(-i_{\text{load}} + D'\tilde{G}_c(K_v e_1 + K_r e_2)). \qquad (5)$$

Using $e_1 = V_{\text{ref}} - V$ and $e_2 = i_{\text{ref}} + \eta e_1 - D'\tilde{G}_c(K_v e_1 + K_r e_2)$, the DC-link voltage in terms of exogenous signals $V_{\text{ref}}, i_{\text{ref}}$ and i_{load} is given by:

$$V = T_{V_{\text{ref}}V} V_{\text{ref}} + G_v T_{i_{\text{ref}}V} (i_{\text{ref}} - i_{\text{load}}) - G_v S i_{\text{load}}, \qquad (6)$$

where $S = [1 + D'\tilde{G}_c K_r + D'\tilde{G}_c G_v(K_v + \eta K_r)]^{-1}$, $T_{V_{\text{ref}}V} = [D'\tilde{G}_c G_v(K_v + \eta K_r)]S$, and $T_{i_{\text{ref}}V} = D'\tilde{G}_c K_r S$. Note that $S + T_{V_{\text{ref}}V} + T_{i_{\text{ref}}V} = 1$, where DC-gains of the above closed-loop transfer functions are given by:

$$|T_{V_{\text{ref}}V}(j0)| = 1, \quad |(G_v T_{i_{\text{ref}}V})(j0)| = \frac{|K_r(j0)|}{|K_v(j0) + \eta K_r(j0)|}$$

$$\text{and} \qquad |(G_v S)(j0)| = \frac{1}{D'(|K_v(j0) + \eta K_r(j0)|)}. \qquad (7)$$

If the load current, i_{load}, is measured and i_{ref} is set to i_{load}, then it follows from (6) that in steady-state $V \approx V_{\text{ref}}$, provided the gain of sensitivity transfer function $G_v S$ at DC is made small. However in the absence of load current measurement, and assuming that at DC, the controller is synthesized to ensure $G_v S$ is small, the steady-state DC-link voltage is given by:

$$V \approx V_{\text{ref}} + \underbrace{\left(\frac{|K_r(j0)|}{|K_v(j0) + \eta K_r(j0)|} \right)}_{\kappa(\eta)} (i_{\text{ref}} - i_{\text{load}}) \qquad (8)$$

Thus in the unmatched case ($i_{\text{ref}} \neq i_{\text{load}}$), the output voltage droops by an amount proportional to the mismatch ($i_{\text{ref}} - i_{\text{load}}$) and the droop-gain.

The outer-controllers K_v and K_r are designed through a *model-based* multi-objective optimization problem. In formulating this problem, we first choose the output variables $z_1 \triangleq W_1 e_1, z_2 \triangleq W_2 e_2, z_3 \triangleq W_3 \hat{u}$, and $z_4 \triangleq W_4 V$ (see Fig. 3) that correspond to weighted (a) tracking error of the DC-link voltage, (b) mismatch between i_{ref} and $D'i_L$, (c) control effort $\hat{u}$, and (d) output voltage tracking, respectively. The optimization problem of interest is to find stabilizing outer-controllers $[K_v \ K_r]^T$ such that the $\mathcal{H}_\infty$-norm of the closed-loop transfer function, T_{wz}, from $w \triangleq [V_{\text{ref}} \ i_{\text{ref}} \ i_{\text{load}}]^T$ to $z \triangleq [z_1 \ z_2 \ z_3 \ z_4]^T$ is minimized. The resulting optimization problem is:

$$\underset{K_v, K_r \in \mathcal{K}}{\arg\min} \|T_{wz}\|_\infty, \qquad (9)$$

where $\mathcal{K}$ is a set of all proper-stabilizing controllers. Weights $W_1(j\omega)$ and $W_2(j\omega)$ are chosen to be large in the frequency range $[0, \omega_{BW}]$ to ensure tracking errors, $e_1 = V_{\text{ref}} - V$, and $e_2 = i_{\text{ref}} + \eta e_1 - D'i_L$, in this frequency range to be small. The design of weight function $W_3(j\omega)$ entails ensuring the control effort lies within saturation limits. The weight function $W_4(j\omega)$ is designed as a high-pass filter to ensure that the transfer function from i_{load} to V is small at high frequencies, which mitigates effects of measurement noise. The optimization problem (9) can be solved efficiently using standard routines [22].

B. Extension to Multi-Converter System

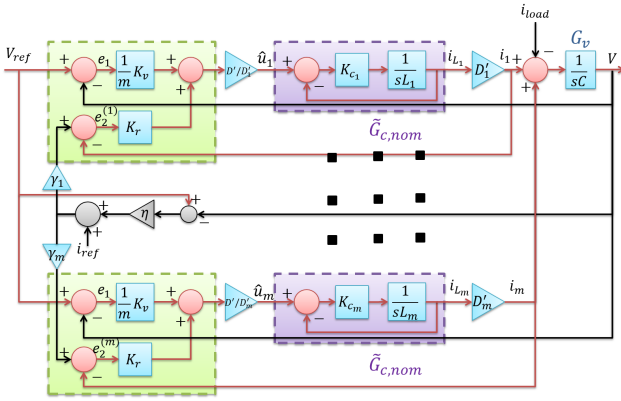In typical architectures, analysis and control synthesis for a parallel network of DC-DC converters is complex,

Fig. 4: A multiple-converters system with shaped inner plants $\tilde{G}_c$. In the proposed implementation, we adopt the same outer controller for different converters, that is, $K_{v_1} = K_{v_2} = .. = K_{v_m} = \frac{1}{m}K_v$ and $K_{r_1} = K_{r_2} = .. = K_{r_m} = K_r$.

and optimal control design becomes untenable even for a moderate number of converters since the complexity scales with the number of converters. We propose a modular controller framework, where we impose structure both within each module and across modules. Here each module comprises a power source along with its DC-DC converter and the corresponding control system (see Fig. 4). This structure significantly simplifies the analysis and synthesis problems for the DC microgrid; both these problems reduce to analyzing and design of an equivalent single converter problem described in Section III-A. This architecture makes optimal control design for multi-converter system tenable since it requires solving the optimization problem only for the equivalent system. We further show that this architecture is robust to perturbations in the assumed structure; for instance if a new module is added that does not follow the structural constraints that we have assumed, the network is still viable in terms of voltage regulation and power sharing between the older sources.

The inter-modular structure is motivated from the observation that the control design for voltage-regulation and reference-current tracking objectives are similar across the modules; accordingly we impose that all the outer-controllers are identical, that is, $K_{v_i} = K_{v_j}$ and $K_{r_i} = K_{r_j}$ for $1 \leq i,j \leq m$ (see Fig. 4). In order to allow for controlled drooping of voltage, the signal $\gamma_k(i_{\text{ref}} + \eta(V_{\text{ref}} - V))$ is fed to the kth outer controller K_{r_k}. The choice of γ_k dictates the power sharing requirements on the kth converter, and since it appears as a reference signal input to the controller, it can be time-varying. We show in Theorem 1 that the proposed implementation distributes the output power nearly in the proportion $\gamma_1 : \gamma_2 : ... : \gamma_m$.

The inner-controllers K_{c_k} are chosen such that the inner-shaped plants from $\hat{u}_k$ to i_{L_k} are identical across k and are given by

$$\tilde{G}_{c,nom}(s) = \left(\frac{\tilde{\omega}}{s + \tilde{\omega}} \right) \left(\frac{s^2 + 2\zeta_{1,nom}\omega_0 s + \omega_0^2}{s^2 + 2\zeta_{2,nom}\omega_0 s + \omega_0^2} \right), \quad (10)$$

where the ratio $\zeta_{1,nom}/\zeta_{2,nom}$ determines the trade-off of 120Hz ripple between the total output current $D'i_L = \sum_{k=1}^{m} D'_k i_{L_k}$ and the capacitor current i_C. For given values of $\zeta_{1,nom}, \zeta_{2,nom}$ and inductance L_k, explicit design of K_{c_k} exists and is given by (4). We further impose that outer-controllers $K_{v_k} = K_v/m$ and $K_{r_k} = K_r$ for all k.

In particular, by our choice of inner and outer controllers, the transfer functions from external references V_{ref}, i_{ref} and i_{load} to the desired output V are identical for all converters. Hence the entire network of parallel converters can be analyzed in the context of an equivalent single converter system. Therefore, $\{K_{v_k}\}$ and $\{K_{r_k}\}$ can be computed by solving $\mathcal{H}_\infty$-optimization problem (as described in Sec. III-A2) similar to the *single* converter case. These design specifications are made precise in the following theorem.

The system representation in Fig. 3 is considered *equivalent* to that in Fig. 4, when the transfer functions from the reference voltage V_{ref}, reference current i_{ref}, load current i_{load} to the DC-link voltage V in Fig. 3 are identical to the corresponding transfer functions in Fig. 4.

Theorem *1:* Consider the single-converter system in Fig. 3 with inner-shaped plant $\tilde{G}_{c,nom}(s)$ given by (10), outer controllers K_v, K_r, droop-coefficient η, and external references $V_{\text{ref}}, i_{\text{load}}, i_{\text{ref}}$; and the multi-converter system described in Fig. 4 with inner-shaped plants $\tilde{G}_{c_k} = \tilde{G}_{c,nom}(s)$ and outer controllers $\left\{K_{v_k} = \frac{1}{m}K_v\right\}$ and $\{K_{r_k} = K_r\}$ for all $k = 1, \ldots, m$, droop-coefficient η, and same external references $V_{\text{ref}}, i_{\text{load}}$ and reference current i_{ref} prescaled by time-varying scalars $\{\gamma_k > 0\}$ for $1 \leq k \leq m$. The following assertions hold:

1. [System Equivalence]: If $\sum_{k=1}^{m} \gamma_k = 1$, then the system representation in Fig. 3 is *equivalent* to the system representation in Fig. 4.

2. [Power Sharing]: For any two converters k and l, $k, l \in \{1, \ldots, m\}$ in a multi-converter system shown in Fig. 4, the difference in the corresponding steady-state scaled output currents is given by:

$$\left| \frac{D'_k i_{L_k}(j0)}{\gamma_k} - \frac{D'_l i_{L_l}(j0)}{\gamma_l} \right| \leq \left(\eta |\tilde{T}_1(j0)| + \left| \frac{1}{\gamma_k} - \frac{1}{\gamma_l} \right| |\tilde{T}_2(j0)| \right) |e_1(j0)|,$$
(11)

where, $\tilde{S}_1 := [(1 + D'\tilde{G}_{c,nom}K_r)]^{-1}$, $\tilde{T}_1 := D'\tilde{G}_{c,nom}K_r\tilde{S}_1$ and $\tilde{T}_2 := D'\tilde{G}_{c,nom}K_v\tilde{S}_1/m$. Furthermore, the steady-state tracking error $e_1 \triangleq V_{\text{ref}} - V$ in DC-link voltage satisfies in the centralized case, where, $i_{\text{ref}} = i_{\text{load}}$,

$$|e_1(j0)| \leq \frac{1}{D'(|K_v(j0) + \eta K_r(j0)|)} |i_{\text{ref}}(j0)|, \quad (12)$$

while in the decentralized case:

$$|e_1(j0)| \leq \frac{|K_r(j0)||i_{\text{ref}}(j0)| + (D'|K_r(j0) + 1)|i_{\text{load}}(j0)|}{D'(|K_v(j0) + \eta K_r(j0)|)}. \quad (13)$$

Proof: See Appendix for details.
Remark 1: If the steady-state tracking error in DC-link voltage is zero, (that is, $|e_1(j0)| = 0$) then from (11), we have perfect output power sharing given by $|D'_1 i_{L_1}(j0)| : \ldots : |D'_m i_{L_m}(j0)| = \gamma_1 : \ldots : \gamma_m$. In practice

the tracking error e_1 is not exactly zero, however, the tracking error is made practically insignificant through an appropriate choice of controllers K_v, K_r with large gains at DC which result from the $\mathcal{H}_\infty$ optimization problem in (9). Moreover, the design of the controllers is such that $|K_v(j0)| < |K_r(j0)|$ resulting in $|\tilde{T}_1(j0)| \leq 1$ and $|\tilde{T}_2(j0)| \leq 1$.

Remark 2: From (11), it is evident that for near equal sharing, that is, $\gamma_k \approx \gamma_l$, for all $k, l \in \{1, \ldots, m\}$, the second term on the RHS in (11) is ≈ 0, thereby resulting in a tighter bound on sharing performance.

Remark 3: The architecture proposed in Fig. 4 also allows for proportional sharing of 120 Hz ripple current among DC sources in a desired ratio. For instance, constraints on the power sources may require that 120 Hz ripple component in the net output current $\sum_k i_k$ must be shared in some specified proportion $\beta_1 : \cdots : \beta_k$. This can be addressed by adjusting reference current i_{ref} command to k^{th} converter as $i_{\text{ref}_k} = i_{\text{ref}} + (\beta_k/\gamma_k)i_{\text{ref},120}$, where $i_{\text{ref},120}$ represents the desired 120 Hz ripple content in total output current.

Remark 4: The droop-like coefficient η controls the trade-off between voltage regulation and power sharing. This is evident from (11)-(13). A sufficiently large value of η ensures small steady-state error in voltage regulation, however, at the expense of *loose* upper bound on power sharing performance reflected through (11).

Remark 5: The proposed control design is also applicable to a mix of converter topologies connected in parallel. This is possible due to identical structure (described in Section II) of different converter models that can be exploited to design identical inner closed-loop plant transfer function $\tilde{G}_c(s)$, and therefore also identical outer-controllers.

IV. SIMULATION RESULTS

In this section, we demonstrate the effectiveness of the proposed approach through simulated case studies. All test cases are simulated in MATLAB/Simulink [22] using SimPower/SimElectronics library. Here, we consider the setup shown in Fig. 5. In order to illustrate the robustness of the proposed approach, the control design assumes nominal (or equivalent single converter) inductance, capacitance and steady-state complementary duty-cycle given by $L = 0.12\text{mH}$, $C = 500\mu\text{F}$ and $D' = V_g/V_{\text{ref}} = 0.5$, whereas the simulated system has non-identical inductances and steady-state complementary duty-cycles. The mismatch (or uncertainty) in L and C parameters is large ($\sim 20\%$). The design parameters for the inner-controller K_c are: damping factors $\zeta_1 = 0.7$, $\zeta_2 = 2.2$, and bandwidth $\tilde{\omega} = 2\pi 300\text{rad/s}$. The outer controllers K_v and K_r are obtained by solving the stacked $\mathcal{H}_\infty$ optimization problem (see Eq. (9)) [11] using appropriate weighting functions.

Results: The controllers derived for the nominal single converter system are used to derive controller parameters for a parallel multi-converter system as described in Sec. III-B (by setting for each converter $K_{v_k} = \frac{1}{m}K_v$ and
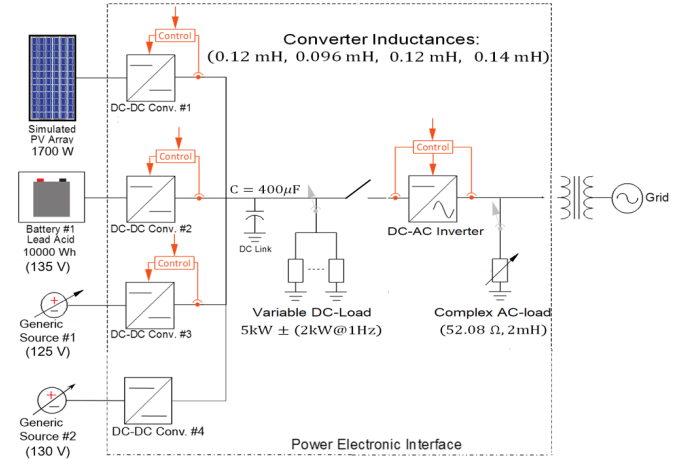

Fig. 5: A parallel network comprising of a PV, a Li-ion battery and two generic sources. It is desired to regulate the DC-link voltage to 250V. The PV module is operated using MPPT algorithm. Its output current, i_{PV}, is directly proportional to the (time-varying) irradiance and is included in our proposed formulation by regarding i_{PV} as part of the disturbance signal, with the net disturbance current modeled as $i_{\text{load}} - i_{\text{PV}}$. The DC-link can additionally be used to power complex AC loads via a DC-AC inverter.

$K_{r_k} = K_r$ for all $k = 1, \ldots, m$). Fig. 6a and Fig. 6c show the voltage regulation at the DC-link to the reference $V_{\text{ref}} = 250V$ for the centralized (i_{load} measurement available) and decentralized implementations. The DC-link load changes by $4kW$ every second ($3kW$ to $7kW$, and $7kW$ to $3kW$). The reference current is considered as $i_{\text{ref}} = 5kW/250V = 20A$. Fig. 6b and Fig. 6d present the results for time-varying sharing. The sources are initially required to provide power in equal proportion, followed by a proportion of $5 : 2 : 3$ from $t = 2s$ onwards. For ease of illustration, the scaled output currents $D'i_L/\gamma$ are plotted. Overlapping values of scaled currents depict excellent sharing performance.

Fig. 6e and Fig. 6f show the results of adding complex AC loads through a DC-AC inverter. The converter system is required to operate in "DC-only" mode until 0.4s. The three DC-sources are required to share their output power in the ratio of $4 : 3 : 3$. The DC-load considered in this test case has a resistance of 20Ω. Subjected to these conditions, the DC-sources regulate the DC-link voltage at 250V (see Fig. 6e), while ensuring desired sharing performance (see Fig. 6f). At $t = 0.4$, the DC-load is dropped and the networked system is interfaced with a complex AC-load $(R,L) = (52.08\Omega, 2\text{mH})$ through a grid-tied DC-AC inverter. Despite this sudden interconnection, the proposed control design facilitates seamless integration to ensure that the average DC-link voltage is regulated at desired 250V, while ensuring the same sharing capabilities. The transient response to grid interconnection remains well within acceptable limits.

Comparison to conventional droop-control scheme: In order to highlight the significance of the proposed approach for excellence in voltage tracking and power sharing, we
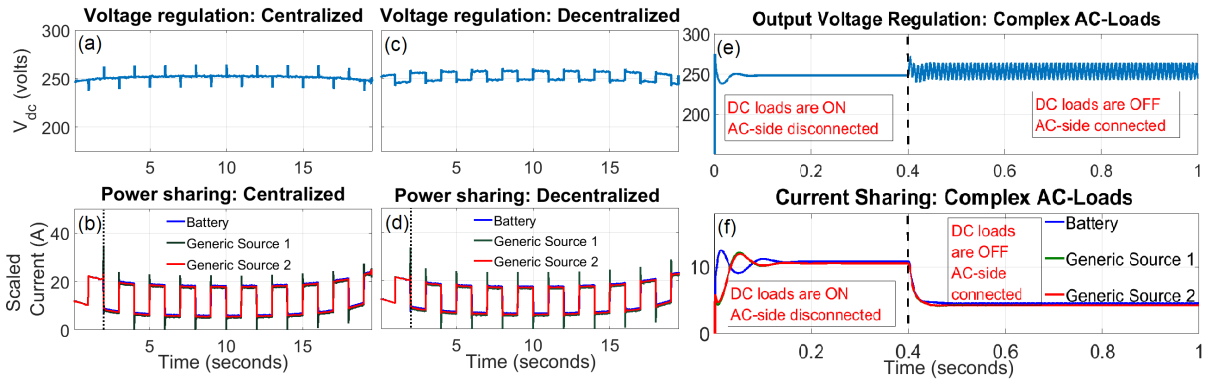
Fig. 6: Simulation results representing centralized control implementation - (a) and (b); decentralized control implementation - (c) and (d); handling of complex AC loads - (e) and (f).
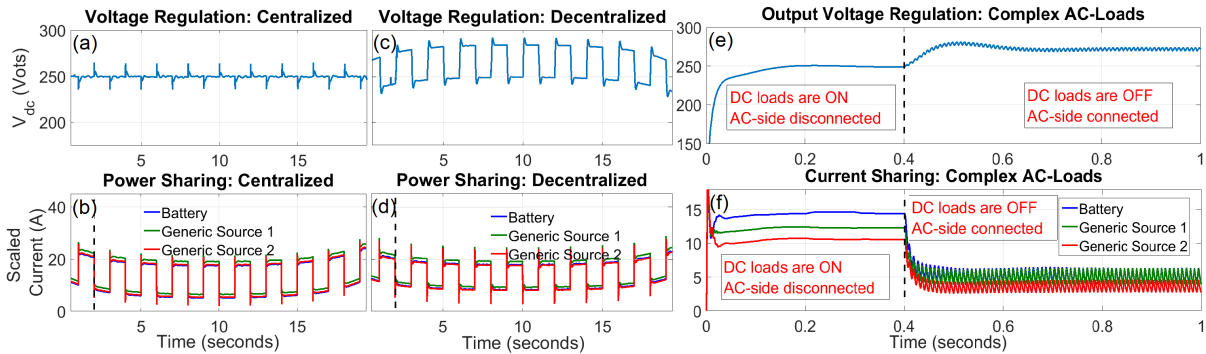

Fig. 7: Simulation results for *droop-based* control design representing centralized control implementation - (a) and (b); decentralized control implementation - (c) and (d); handling of complex AC loads - (e) and (f). Compared to the proposed implementation, the droop-based design is sluggish and has considerably poor steady-state voltage tracking behavior in all the scenarios.

simulate the microgrid setup in Fig. 5 using conventional droop-based control scheme. In particular, we use the inner-outer control architecture with PI compensators for both inner as well as outer loops and a droop-law on the outer-voltage loop. The PI compensators and droop gains are appropriately tuned to achieve desirable voltage regulation and power sharing performance.

Fig. 7 shows the performance of droop-based design for the the simulation setup shown in Fig. 8. While in the centralized implementation (load current is known) in Figs. 7a and 7b the droop-based design results in similar tracking and power sharing performance as indicated in Figs. 6a and 6b where the control design proposed in this manuscript is implemented; however, results for decentralized implementation of droop scheme in Figs. 7c and 7d are quite unsatisfactory. Here, variations in output voltage are large due to periodic change in output load at the DC-link where the difference between the maximum and minimum output voltages during the course of simulation is almost 60V. On the other hand, the control design proposed here results in excellent voltage tracking performance even for the decentralized implementation (see Fig. 6c).

We further evaluate the performance of droop controller for scenarios that capture interfacing DC-side with complex AC loads (see Figs. 7e and 7f). Compared to voltage tracking in Fig. 6e using the proposed approach,

the droop-based scheme is sluggish and result in poor steady-state behavior. This is expected since as the proposed scheme incorporates the bandwidth requirements on voltage tracking through an optimization framework described in (9), where high-bandwidth (faster response) is encoded through appropriate choice of weighting transfer functions. Moreover, the sharing performance for the droop-based scheme is unsatisfactory in Fig. 7f when compared to its counterpart in Fig. 6f. The results also signify the necessity of an inner-outer control architecture over a single-loop design. Through an appropriate choice of inner-loop controller in the proposed design (see (4)), the ripple in inductor currents are traded-off for ripple in DC-link voltage in Fig. 6e. On the other hand, while designing the droop-based controllers, we restrict ourselves to conventional PI controllers where such trade-off are not easily handled. Thus a separate inner-outer control design allows for greater flexibility and desirable decoupling behavior between voltage and current tracking.

V. EXPERIMENTAL VALIDATION

To verify the effectiveness of the proposed approach, a test rig with three parallel operated DC sources and a parallel PV simulator PVS60085MR is built (see Fig. 8). It is desired to regulate the DC-link voltage to $V_{\mathrm{ref}} = 60$V.
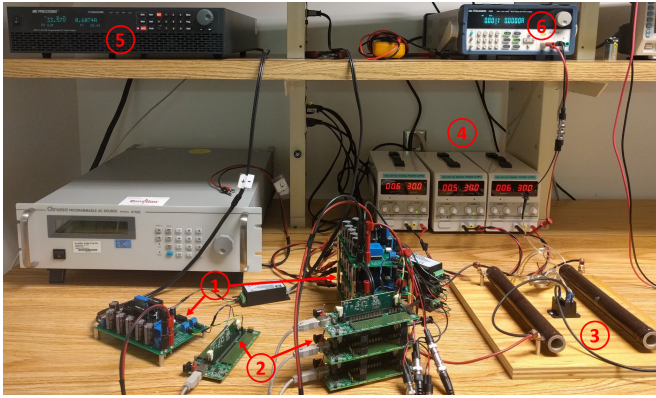
Fig. 8: Experimental setup with (1) custom-designed boost-converter boards, (2) controllers implemented on TMS320F28335 Delfino MCUs, (3) variable load - two resistors, each of value 50Ω, (4) DC-sources with maximum rated output voltage of 30V, (5) PV simulator subjected to simulated noisy ramp profile with a peak power of 43W and controlled using MPPT algorithm , and (6) relay for load.

System Performance: The controllers for a *nominal* single-converter system are designed using the multi-objective robust optimal control framework described in Sec. III-A and is extended to a three-converter system using the methodology described in Sec. III-B. The details of weighting transfer functions and the resulting controller transfer functions are provided in the Appendix. In order to analyze robustness to modeling uncertainties, a 50% uncertainty in capacitance is considered. For brevity, case studies pertaining only to more challenging decentralized scenario are reported; where total load current i_{load} is *unknown* and there is no communication among the controllers. Furthermore, PV is regarded as a current source and injects power directly at the DC-link, as described in Sec. IV. Since, the load current is unknown, constant $i_{\text{ref}} = 2A$ is used.

Case A: Power sharing when PV is off: Figures 9a and 9c show that power from the DC sources get distributed respectively in ratios $1 : 1 : 1$ and $2 : 1 : 1$, irrespective of the load at the DC-link; even when there are load changes as high as 100%. Figures 9b and 9d illustrate excellent DC-link voltage regulation at $V_{\text{ref}} = 60V$ in absence of communication between controllers about load. The regulation error is within 1V even when load is changed by 100%.

Case B: Power sharing with PV on: We now evaluate the performance of our control design under additional uncertainty in power generation, that is, a PV source under simulated noisy ramp irradiance profile is connected at the DC-link. The converter controllers to generic DC-sources are agnostic to PV output. The inclusion of PV also tests the robustness of the system to load disturbances since PV current can be viewed as time varying uncertain load at the DC-link for the rest of the power sources. Fig. 9e shows that DC sources adequately compensate for the PV disturbance, that is, they exhibit power profile *complementary* to PV profile, even though the loading conditions are not communicated to the

controllers; also DC-link voltage is well regulated (see Fig. 9f).

Case C: Resilient to unforeseen failure in power generation in an agnostic setup: Robust performance of the networked system is now evaluated for the scenario when one of the generic DC sources is abruptly turned OFF (mimicking a power source failure in a network). Furthermore, this information is not communicated to the network. If this information were communicated, our architecture in Sec III-B, will make the following changes - 1) The outer controllers $K_{v_k} = (1/m)K_v$ will be updated to $K_{v_k} = K_v/(m-1)$, and 2) $\sum \gamma_k$ will be readjusted to sum up to 1 for the active sources. However, even without this communication and edits, Fig. 9g shows that as the DC-source #2 is abruptly turned OFF, the net power output from other DC sources auto-adjusts to loss in power generation from DC-source #2, and ensures DC-link voltage regulation (Fig. 9h) and equal power sharing (Fig. 9g). Furthermore, at $t = 4.3s$, load R_2 is shed, while DC-source #2 is still inactive. Despite the generation and load uncertainties, DC-link voltage is maintained within the viable limits and the load power is shared equally by the active sources.

APPENDIX

A. Proof of System Equivalence

Proof: The *system equivalence* results directly from choice of the control architecture. For the single converter system in Fig. 3 with inner-shaped plant $\tilde{G}_c(s) = \tilde{G}_{c,nom}(s)$, the mismatch e_2 in the current signal (input signal to controller K_r) is given by

$$e_2 = i_{\text{ref}} + (\eta - D'\tilde{G}_{c,nom})e_1 - D'\tilde{G}_{c,nom}K_r e_2. \tag{14}$$

For the networked system in Fig. 4, the error in the DC-link voltage regulation is given by $e_1^{(k)} = V_{\text{ref}} - V \triangleq e_1$. If we denote the total mismatch in current signal by e_2, that is, $e_2 = \sum_{k=1}^{m} e_2^{(k)}$, then from Fig. 4,

$$\underbrace{\sum_{k=1}^{m} e_2^{(k)}}_{e_2} = \sum_{k=1}^{m} \gamma_k[i_{\text{ref}} + \eta e_1] - D'\tilde{G}_{c,nom}\left(K_v e_1 - K_r \underbrace{\sum_{k=1}^{m} e_2^{(k)}}_{e_2}\right). \tag{15}$$

Since $\sum_k \gamma_k = 1$, the above equation reduces to (14). Thus, the transfer function from exogenous signals to current mismatch is identical for the two systems. Similarly, the tracking error in DC-link voltage regulation for the two systems is given by $V_{\text{ref}} - V$. Finally, the multi-converter system, the voltage at the DC-link is derived as $V = G_v(-i_{\text{load}} + D'\tilde{G}_{c,nom}(K_v e_1 + K_r e_2))$, which is again identical to (5) for single-converter system. Moreover, since the expressions for error signals e_1 and e_2 in terms of exogenous signals $V_{\text{ref}}, i_{\text{ref}}$ and i_{load} are identical for the two systems, the expressions for DC-link voltage V have identical forms for the two systems. This establishes the required *equivalence* between the two systems. ∎
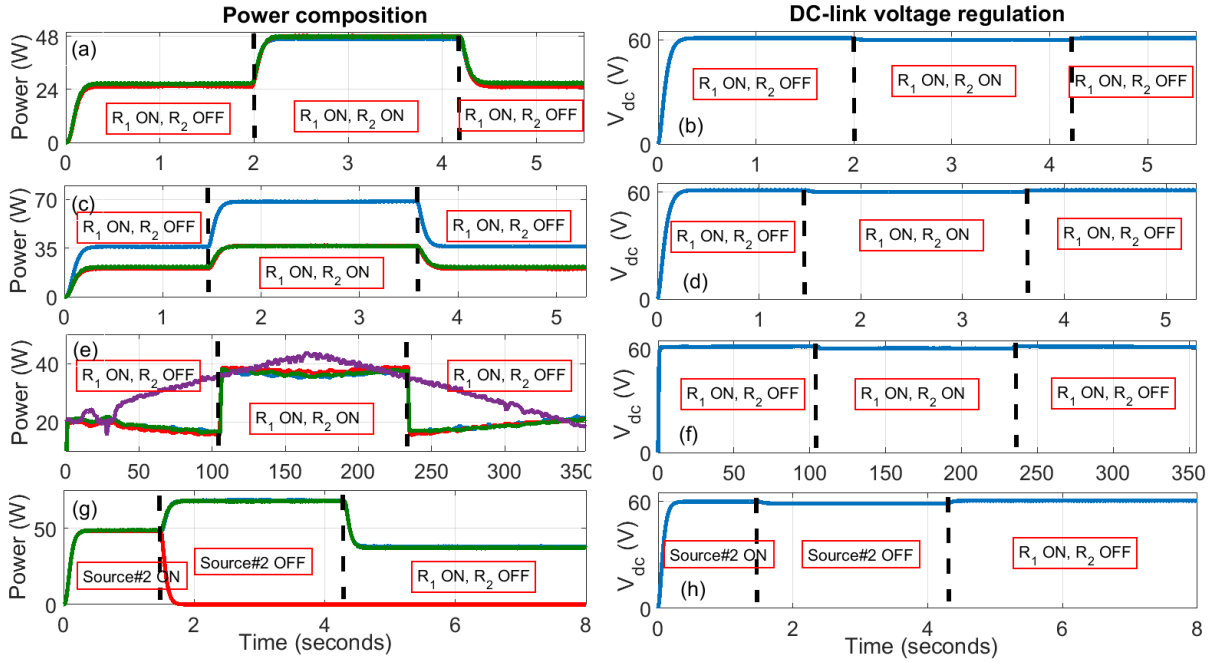
Fig. 9: Experimental results demonstrating effectiveness of the proposed control design under perfectly decentralized implementation for several test scenarios: 1:1:1 sharing (PV off) - (a) and (b); 2:1:1 sharing (PV off) - (c) and (d); 1:1:1 sharing (PV on) - (e) and (f); Equal sharing in presence of abrupt failure in power generation - (g) and (h). Colors blue, red, green and purple indicate power outputs of DC sources 1, 2, 3 and PV emulator, respectively.
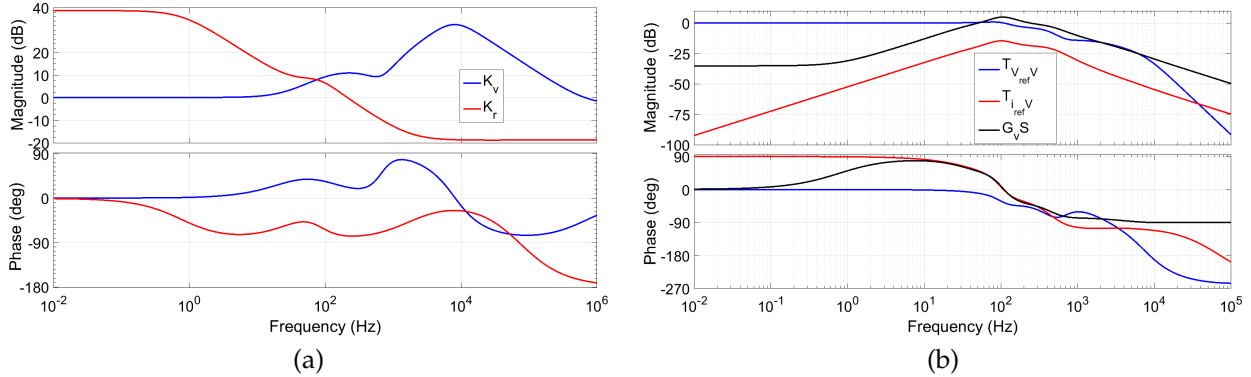

Fig. 10: Magnitude and phase responses of (a) controller transfer functions K_v and K_r, (b) sensitivity and complementary sensitivity transfer functions.

B. Proof of Power Sharing

Proof: Using (15), the mismatch in the current signal for k^{th} converter is given by $e_2^{(k)} = \gamma_k \tilde{S}_1 i_{\text{ref}} + (\gamma_k \eta - \frac{D'}{m} \tilde{G}_{c,nom} K_v) \tilde{S}_1 e_1$. From Fig. 4, the output current $i_k = D'_k i_{L_k}$ for the kth converter is given by $i_k = D' \tilde{G}_{c,nom} \left[\frac{1}{m} K_v e_1 + K_r e_2^{(k)} \right]$. Therefore,

$$\left| \frac{i_k(j0)}{\gamma_k} - \frac{i_l(j0)}{\gamma_l} \right| \leq \left(\eta |\tilde{T}_1(j0)| + \left| \frac{1}{\gamma_k} - \frac{1}{\gamma_l} \right| |\tilde{T}_2(j0)| \right) |e_1(j0)|$$

The expressions for the bounds on the tracking error for the two scenarios is directly obtained from (6) and the *system equivalence* described earlier. ∎

C. Weighting Functions and Controller Parameters

The weighting transfer functions W_1, W_2, W_3 and W_4 are chosen to reflect design and performance specifi-cations. In our experiments, we have considered the following weighting transfer functions:

$$W_1 = 0.4167 \frac{(s + 452.4)}{(s + 1.885)}, \qquad W_2 = 0.4167 \frac{(s + 1206)}{(s + 5.027)},$$

$$W_3 = 0.04, \qquad W_4 = 37.037 \frac{(s + 314.2)}{(s + 3.142 \times 10^4)}.$$

Weight W_1 is chosen to be large in the frequency range $[0, 30]$Hz so that the sensitivity transfer function corresponding to error in voltage tracking is small in that frequency. Note that from (5), the error in voltage tracking is given by:

$$e_1 := V_{\text{ref}} - V$$
$$= \underbrace{\left(1 - T_{V_{\text{ref}} V} \right) V_{\text{ref}} - G_v T_{i_{\text{ref}} V} \left(i_{\text{ref}} - i_{\text{load}} \right)}_{S_{V_{\text{ref}} V}} + G_v S i_{\text{load}}.$$

One of the objectives of the optimal control problem in (9) is to minimize the norm of weighted error sensitivity transfer function $W_1 S_{V_{\mathrm{ref}}V}$. Since W_1 is shaped as a low-pass filter, which gives high weight at low frequencies and relatively low-weights at high frequencies, the optimal solution is such that $S_{V_{\mathrm{ref}}V}$ is small at low frequencies. A small value of the sensitivity transfer function $S_{V_{\mathrm{ref}}V}$ translates to a small error in voltage tracking from above equation. Similarly, W_2 is chosen to be large in the frequency range $[0,80]$Hz so that the transfer function from mismatch between the sourced output current and the reference current to the regulation error e_1 is small. Note that the bandwidth of W_2 is chosen to be larger than the bandwidth of W_1, primarily to allow for faster dynamics in the inner current loop since change in capacitor voltage occurs at a relatively slower timescale than a sudden change in the loading conditions. By satisfying this condition, the reference value of the inner loop which is the output of the outer controller can be considered relatively constant (see Fig. 3). W_3 is chosen to be constant and is designed to make the control effort lie within the limits at all frequencies. Finally, W_4 is designed as a high-pass filter to ensure that the transfer function from i_{load} to V is small at high-frequencies, which mitigates effects of high-frequency measurement noise. The corresponding outer controllers K_v and K_r are obtained by solving a multi-objective $\mathcal{H}_\infty$-optimization problem in (9). The controller orders are then reduced using balanced truncation [12] for efficient implementation:

$$K_v = 0.69 \frac{(s+4.42e10^6)(s+167)(s^2+3930s+1.75e10^7)}{(s+4891)(s+719.2)(s^2+7.21e10^4s+2.51e10^9)}$$

$$K_r = -0.12 \frac{(s-4.56\times10^5)(s+1.12\times10^4)}{(s+4.64\times10^5)(s+4.96)}$$
$$\times \frac{(s+355.7)(s+248.9)}{(s^2+714.9s+2.66\times10^5)}$$

Fig. 10 shows the bode plots of the sensitivity and complementary sensitivity transfer functions described in (6). The DC-gains for these transfer functions are:

$$|(G_v S)(j0)| = 0.0182, \quad |T_{V_{\mathrm{ref}}V}(j0)| = 1, \quad |T_{i_{\mathrm{ref}}V}(j0)| = 0.$$

As a consequence, we achieve the desired control objectives of $|T_{V_{\mathrm{ref}}V}(j0)| = 1$ and $|(G_v S)(j0)| \approx 0$. The resulting droop-gain $\kappa(\eta)$ is evaluated to be 0.7822.

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