Droopless Active and Reactive Power Sharing in Parallel Operated Inverters in Islanded Microgrids

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***Abstract*— Microgrids have emerged as viable alternatives for supporting the utility grid, reducing feeder losses and improving power quality by enabling integration of growing deployments of distributed energy resources (DERs) with local loads. They are capable of operating in both grid-tied as well as islanded modes. There are two primary objectives in the islanded mode of operation of microgrids - (a) ensuring system stability by regulating the voltage and frequency at the point-of-common-coupling (PCC), and (b) load power sharing among multiple DERs connected in parallel. While conventional droop based schemes enjoy the advantages of fully decentralized implementation (no communication) and plug-and-play capabilities, such schemes often fail to address the issue of precise active and reactive power sharing, primarily due to unmatched impedances and different ratings of DERs. In this paper, we overcome this limitation by proposing a novel, *droopless* control scheme for accurate active and reactive power sharing among DERs in an islanded microgrid, while simultaneously regulating output voltage and frequency at the PCC. Similar to droop based schemes, the proposed method too facilitates fully decentralized implementation. This is achieved as a consequence of a smart choice of control design enabled by - (a) disturbance rejection viewpoint, (b) decoupling of $d-q$ control loops through appropriate feedforward blocks, and (c) extension of the network control scheme proposed in our prior work [1]. A system consisting of three parallel inverters is simulated in MATLAB Simscape environment for various challenging scenarios and the results corroborate the effectiveness of the proposed approach.**

I. INTRODUCTION

The North American electrical grid is regarded as the most significant engineering achievement of the 20th century [2], however, the infrastructure that defines the U.S. electric grid is based largely on pre-digital technologies and is ill-equipped to serve smaller, innovative solar or wind facilities. However, the increasing use of renewable generation and distributed energy resources (DERs), such as residential solar and home energy storage, along with customers changing energy usage patterns lead to greater uncertainty and variability in the electric grid. In this regard, *microgrids* [3] are hypothesized as viable alternatives for supporting a flexible and efficient electric grid by enabling the integration of growing deployments of distributed energy resources such as renewables like solar and wind. In addition, the use of local sources of energy to serve local loads helps reduce energy losses in transmission and distribution, further increasing efficiency of the electric delivery system. Fig. 1 represents a schematic of a microgrid. In such microgrids, multiple DC sources, connected in parallel through power electronic converters, provide power at their common output, the AC-link (also known as the point of common coupling (PCC)) at a desired voltage magnitude and frequency. Parallelization of power sources enables high system reliability, higher power output, and plug-and-play capability.

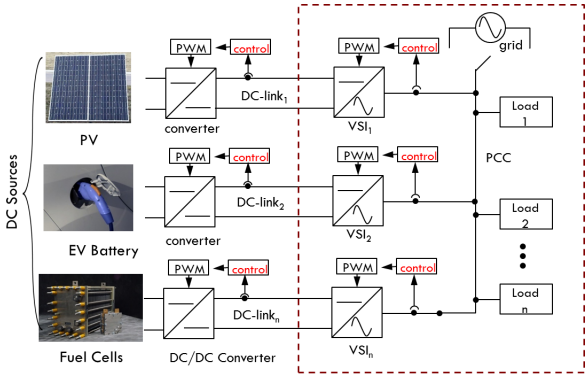

Fig. 1: A schematic of a microgrid. An array of DC power sources provide power at the respective DC-links, where the voltage is regulated by DC/DC converters. A network of parallel inverters that connect to the DC-links convert the total current from the sources at the regulated voltage to alternating current (AC) at its output to satisfy the power demands of the AC loads.

Microgrids can be operated in both grid-tied or islanded mode. In the grid-tied mode, a microgrid is connected to the utility grid through a tie line at the PCC; voltage and frequency at the PCC are regulated by the grid. In islanded mode of operation, DERs mainly provide power to local loads through local control. Note that the islanded operation is particularly challenging since it requires regulating the desired voltage and frequency at the PCC. Islanded mode of operation is further classified into two commonly practiced control design methodologies [4]: (a) *Single-master operation*: In this control architecture, a single *master* voltage source inverter (VSI) is employed to regulate the voltage and frequency at the PCC, while other VSIs operate in current/power injection mode and provide prespecified powers at the PCC. While this mode of operation inherits a relatively simple control architecture, it does so at the cost of admitting a single point of failure at the master VSI. (b) *Multi-master operation*: In multi-master configuration, the control design at *every* VSI has a combined objective to regulate voltage and

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frequency at the PCC, while ensuring prespecified active and reactive power sharing at the PCC.This architecture avoids single point of failure; however at the cost of increased complexity of the control design. In this manuscript, we propose a novel control methodology that enjoys the best of both worlds. On one hand the design is structurally robust due to choice of multi-master mode of operation, while on the other hand each VSI admits a simple control design.

Apart from maintaining voltage and frequency at the PCC, it is also desired for DERs to share their active and reactive powers simultaneously in order to ensure stability and economical operation of microgrids [5]. Conventional droop-based schemes are the well-developed control schemes that facilitate decentralized control implementation as they do not require any communication lines. Droop control can be used to achieve active and reactive power sharing by imitating the steady-state characteristics of synchronous generators (SGs) in microgrids [6]. However, conventional droop schemes fail to address the issue of precise active and reactive power sharing, primarily due to unmatched impedances and different ratings of DERs. The major shortcoming of droop-based schemes is precisely this fundamental trade-off between voltage and frequency regulation, and power sharing. Moreover, droop control schemes result in slow dynamic responses, primarily due to their association with steady-state behavior of SGs.

While the inertia of DERs can be enhanced though virtual synchronous generator (VSG) control method compared to the droop control, the output active power of VSG is oscillatory and virtual inertia results in sluggish dynamic power sharing [7]. When all DERs operate at the same frequency in the steady-state conditions, the active power is regulated well in improved droop control schemes, however the sharing performance in reactive power is still poor and results in harmonic power injections in DERs under unmatched feeder impedance and nonlinear loading conditions [8]. In the worst case scenario, poor reactive power sharing may result in large circulating reactive powers among DERs, resulting in system instability [9]. Another undesirable characteristic of droop-based control schemes is their dependence on line impedance (i.e., $Q-V$ and $P-\theta$ droop control strategy is used in inductive line, and $Q-\theta$ and $P-V$ droop control strategy is used in resistive lines) [10]. Moreover, the droop method results in system instability when the slope of the droop characteristics is small [11].

While an inverter-level stability and performance analysis can be obtained in detail, there is hardly any literature on analyzing stability and performance at the microgrid level, precisely due to availability of only *local* measurements in decentralized control designs [12]. Moreover, the power demanded at the PCC is uncertain and time-varying. Typical approaches to address the problem of voltage (and frequency) regulation in presence of unknown loads include either using adaptive control [13], which often requires knowledge of nominal load power, or by letting the voltage and frequency droop in a controlled manner, which inherits the problems of droop-based designs described above.

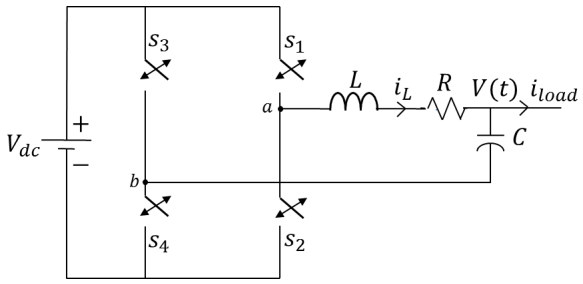

Fig. 2: Circuit representing a full-bridge inverter. The AC-side current is given by i_{load}. The switches s_1, s_2, s_3 and s_4 control the AC-side voltage $V(t)$.

In this manuscript, we overcome the aforementioned limitations by proposing a scalable, decentralized, *droopless* control framework for precise active and reactive power sharing through a carefully chosen structured control architecture. The architecture finds its genesis through three fundamental steps - (a) *disturbance rejection viewpoint*: The problem of voltage (and frequency) regulation in presence of uncertain, time-varying loads is posed as a disturbance-rejection problem, where the load current is regarded as an external disturbance signal. Controllers are synthesized such that the transfer function gain from disturbance to output voltage is small. This viewpoint also enables to incorporate nonlinear loads into the network without a need to measure the load current separately. (b) *decoupled control loops*: The requirements for active and reactive power sharing is imposed as two decoupled control problems through an appropriately chosen feed-forward decoupling terms. (c) *extension of network control approach*: In this work, we build upon the power sharing controller for DC-DC converters in our prior work [1] and extend this architecture to a network of parallel VSIs. This extension is shown to overcome the limitations of droop-based control schemes, while retaining its useful features, such as decentralization. Moreover, through an appropriate choice of compensators, stability and performance of entire network of parallel inverters is analyzable in terms of an *equivalent* single inverter system, as remarked in Theorem 1.

II. PRELIMINARIES: MODELING OF INVERTERS

This section describes the *cycle*-averaged dynamical models of full-bridge DC-AC inverters, which transform sources of direct current (DC) to equivalent sources of alternating current (AC). The dynamical models are derived using a disturbance-rejection viewpoint, where the load current (and the associated load dynamics) is regarded as a disturbance signal and a control design is sought to efficiently reject the disturbance.

Fig. 2 shows the schematic of a full-bridge DC-AC inverter. A full-bridge inverter [14] consists of two two legs containing two switches each - (a) s_1 and s_2, (b) s_3 and s_4. The AC-side load is interfaced thorough an RL branch to the full-bridge inverter, where R and L represent the internal resistance and inductance of the interface branch, respectively. The interface reactor also acts as a low-pass

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filter and ensures low-ripple AC-side current i_L resulting from switching the semiconductor switches. The voltages at terminals a and b are denoted by periodically switching ON/OFF the switches s_1/s_2 and s_3/s_4, respectively. The quantities V_{dc}, V and i_{load} denote the DC-side voltage, AC-side voltage and AC-side load current, respectively. If switch s_1 is ON (s_2 is OFF) for d_a proportion of time during a switching cycle, the average voltage at terminal a is given by $V_a(t) = d_a(t)V_{\text{dc}}$. $d_a(t)$ is also referred as *duty-cycle* of switch s_1. Similarly, the average voltage at terminal b is given by $V_b(t) = d_b(t)V_{\text{dc}}$, where $d_b(t)$ denotes the duty-cycle of switch s_3. Thus, by combining the two states of operation, the cycle-averaged dynamical model of a full-bridge DC-AC inverter is given by:

$$\begin{aligned} L\frac{di_L(t)}{dt} + Ri_L(t) &= \underbrace{(d_a(t) - d_b(t))\, V_{\text{dc}} - V(t)}_{u(t):=m(t)V_{\text{dc}} - V(t)} \\ C\frac{dV(t)}{dt} &= i_L(t) - i_{\text{load}}(t), \end{aligned} \tag{1}$$

where the control signal $u(t) = m(t)V_{\text{dc}}$ represents the average voltage between terminals a and b. $m(t) \in [-1, 1]$ is the modulating signal and is related to the difference in duty-cycles at terminals a and b. Note that for a given value of modulating signal, there are infinitely many choices for the duty-cycles $d_a(t)$ and $d_b(t)$. We address this non-uniqueness by considering the following switching scheme:

	$m(t) \geq 0$	$m(t) < 0$
$d_a(t)$	$m(t)$	0
$d_b(t)$	0	$-m(t)$

Note that (1) represents the dynamics of an inverter in the fixed-frame (or $\alpha - \beta$ frame [14]). Let ω denote the frequency of the desired sinusoidal voltage signal. For the reasons described later, it is useful to consider the dynamics in the rotating ($d-q$ frame [14]). Remark that any alternating signal $\overrightarrow{f}$ in the fixed frame can be represented as $\overrightarrow{f} = (f_d + jf_q)e^{j\theta(t)}$, where f_d and f_q denote the $d-q$ components of the signal $\overrightarrow{f}$, and $\theta = \theta_0 + \int \omega(\tau)d\tau$ is the angle of rotation. Dynamics of a full bridge-inverter in the $d-q$ frame can be expressed as:

$$\begin{aligned} L\frac{di_d(t)}{dt} &= \underbrace{L\omega(t)i_q(t) + m_d(t)V_{\text{dc}} - V_d(t)}_{\tilde{u}_d} - Ri_d(t) \\ L\frac{di_q(t)}{dt} &= \underbrace{-L\omega(t)i_d(t) + m_q(t)V_{\text{dc}} - V_q(t)}_{\tilde{u}_q} - Ri_q(t) \\ C\frac{dV_d(t)}{dt} &= C\omega(t)V_q(t) + i_d(t) - i_{\text{load},d}(t) \\ C\frac{dV_q(t)}{dt} &= -C\omega(t)V_d(t) + i_q(t) - i_{\text{load},q}(t), \end{aligned} \tag{2}$$

where $[i_d,\ i_q], [V_d,\ V_q], [i_{\text{load},d},\ i_{\text{load},d}]$ and $[m_d,\ m_q]$ denote the $d-q$ components of i_L, V, i_{load} and m respectively. The instantaneous real (P) and reactive (Q) powers of an inverter are given by:

$$\begin{aligned} P(t) &= V_d(t)i_d(t) + V_q(t)i_q(t), \\ Q(t) &= -V_d(t)i_q(t) + V_q(t)i_d(t). \end{aligned} \tag{3}$$

In an islanded mode of operation, it is desired to regulate the voltage at the output to some reference signal $\hat{V}\cos(\theta(t))$. This requirement can be imposed by considering $V_{\text{ref},d} = \hat{V}$ and $V_{\text{ref},q} = 0$. This choice of $d-q$ components facilitates the following constraints on reference powers and currents, i.e., from (3), we obtain:

$$P_{\text{ref}} = \hat{V}i_{\text{ref},d}, \qquad Q_{\text{ref}} = -\hat{V}i_{\text{ref},q}. \tag{4}$$

Thus the requirements on active and reactive powers are directly enforced by imposing requirements on $d-q$ coordinates of the inductor current. Note that from (2), the dynamics of i_d and i_q are mutually coupled. However, an architecture that facilitates decoupled dynamics of i_d and i_q is preferred for efficient regulation of active and reactive powers. This can be achieved through an appropriately chosen feed-forward term that decouples the $d-q$ components of the inductor current, and thus forms the basis of the control design proposed in this work. In the next section, we describe the control design of a single DC-AC inverter in detail.

III. CONTROL OF SINGLE INVERTER

In islanded mode of operation, the goal of control design is to regulate the AC-link voltage. This is achieved through an equivalent control of the modulating signal $m_d(t)$ and $m_q(t)$ in (2). However, for the purpose of control design and implementation, one must focus directly on the control inputs $\tilde{u}_d(t)$ and $\tilde{u}_q(t)$, which in turn determine the modulating signals $m_d(t)$ and $m_q(t)$. Due to presence of $L\omega$ term in (2), dynamics of i_d and i_q are coupled. To decouple the dynamics, m_d and m_q can be defined as:

$$\begin{aligned} m_d &= \frac{\tilde{u}_d - L\omega i_q + V_d}{V_{\text{dc}}} \\ m_q &= \frac{\tilde{u}_q + L\omega i_d + V_q}{V_{\text{dc}}}, \end{aligned} \tag{5}$$

The objective of voltage regulation is achieved using a nested inner-current outer-voltage control architecture shown in Fig. 3a. Note that (2) indicates that V_d and V_q are also coupled and thus the inverter system is a multi-input-multi-output (MIMO) system. Similar to the decoupling in current dynamics, coupling between V_d and V_q is eliminated by a decoupling feed-froward compensation. This decoupling makes it possible to control V_d by $i_{\text{ref},d}$ and V_q by $i_{\text{ref},q}$. Fig. 3b, which is more insightful for control design, shows two decoupled single-input-single-output (SISO) control loops. With reference to Fig. 3a, $i_{\text{ref},d}$ and $i_{\text{ref},q}$ are determined as:

$$\begin{aligned} i_{\text{ref},d} &= u_d - C(\omega V_q) \\ i_{\text{ref},q} &= u_q + C(\omega V_d), \end{aligned} \tag{6}$$

where u_d and u_q are two new control inputs. In the inner-outer control architecture, outer (voltage) compensators K_v generate control signals u_d and u_q that are effectively

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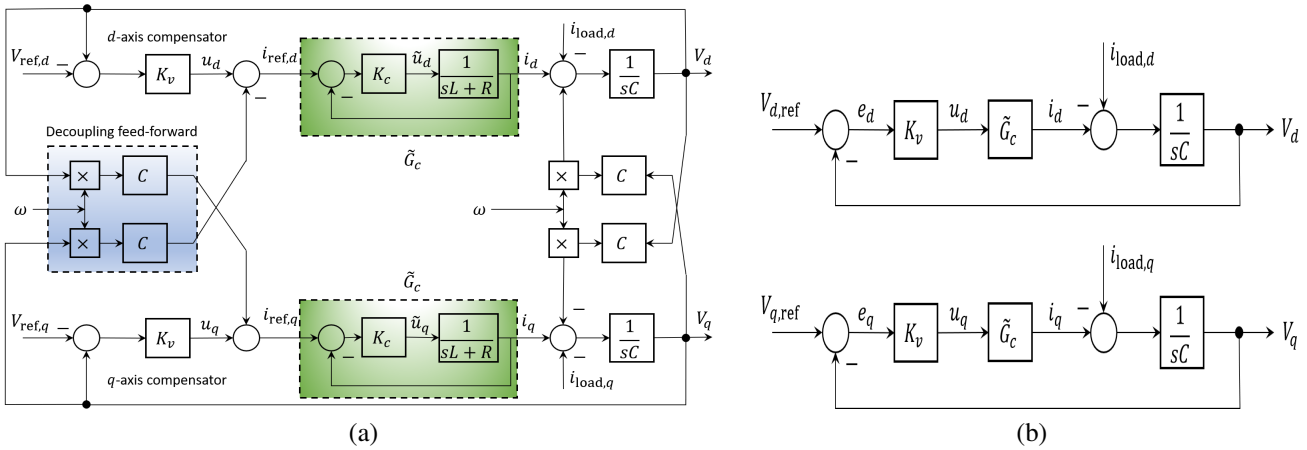

Fig. 3: (a) Control model of a single full-bridge DC-AC inverter. The feed-forward term decouples the dynamics of i_d and i_q. (b) Control model with decoupled loops.

mapped to references of inner (current) loops shown by $\tilde{G}_c$ in Fig. 3. Inner controllers K_c are used to regulate the $d-q$ components of inductor currents to references $i_{\text{ref},d}$ and $i_{\text{ref},q}$, respectively. We use $\tilde{G}_c \triangleq 1/(sL+R)$ and $G_v = 1/sC$ to denote the inner and outer open-loop plants, respectively.

The inner controller K_c is chosen such that the inner closed-loop plant $\tilde{G}_c$ behaves as a simple first-order low-pass filter with cut-off frequency τ^{-1}. The low-pass behavior ensures mitigation of high-frequency noise. In particular, we adopt the following PI control design for inner controller:

$$K_c(s) = \frac{1}{\tau}\left(L + \frac{R}{s}\right), \tag{7}$$

which results in inner closed-loop transfer function:

$$\tilde{G}_c(s) = \frac{G_c(s)K_c(s)}{1+G_c(s)K_c(s)} = \frac{1}{\tau s+1}. \tag{8}$$

The outer-controller K_v is chosen as another PI compensator to reflect design specifications, such as fast voltage regulation, zero voltage tracking error and robustness to parametric uncertainties. Let K_v be given by:

$$K_v(s) = k\frac{s+z}{s}. \tag{9}$$

From Fig. 3b, the loop gain is given by:

$$l(s) = K_v(s)\tilde{G}_c(s)G_v(s) = \frac{k}{\tau C}\left(\frac{s+z}{s+\tau^{-1}}\right)\frac{1}{s^2}. \tag{10}$$

Note that the double integrator introduces a -180° phase delay at low frequencies, i.e., $\angle l(j\omega) \approx -180^\circ$ at low frequencies. If $z < \tau^{-1}$, then $\angle l(j\omega)$ first increases until it reaches its maximum value, δ_m, at a frequency ω_m. Beyond ω_m, $\angle l(j\omega)$ decreases until it asymptotically approaches -180°. δ_m and ω_m are related to z and τ^{-1} as:

$$\delta_m = \sin^{-1}\left(\frac{1-\tau z}{1+\tau z}\right), \text{ and } \omega_m = \sqrt{z\tau^{-1}}. \tag{11}$$

At gain-crossover frequency ω_c the magnitude of loop gain must be unity, i.e., $|l(j\omega_c)| = 1$. In our design, we choose $\omega_c = \omega_m$, then the unity loop gain condition translates to

$$k = C\omega_m. \tag{12}$$

In order to determine the location of compensator zero z, we use the method of *symmetrical optimum* [15], which is suitable for a loop gain with double integrator poles. In fact, if the phase margin is chosen as 53°, i.e., $\delta_m = 53^\circ$, it can be shown that the closed-loop plant $l(s)/(1+l(s))$ has triple poles at $s = -\omega_m$. Moreover, a phase margin of $\delta_m = 53^\circ$ ensures high robustness margin for the closed-loop system and is reflected in our evaluations in Sec. V. Thus with appropriate feed-forward compensations, the inverter dynamics is effectively decoupled into two separate control loops. Here each loop admits an inner-outer control architecture with relatively simple choice of inner and outer compensators as described in (7) and (9), respectively. Note that for the system shown in Fig. 3b, $d-q$ components of the output voltage are given by:

$$V_d = \underbrace{\left(\frac{G_v\tilde{G}_cK_v}{1+G_v\tilde{G}_cK_v}\right)}_{T(s)}V_{\text{ref},d} - \underbrace{\left(\frac{G_v}{1+G_v\tilde{G}_cK_v}\right)}_{G_v(s)S(s)}i_{\text{load},d}$$

$$V_q = \left(\frac{G_v\tilde{G}_cK_v}{1+G_v\tilde{G}_cK_v}\right)V_{\text{ref},q} - \left(\frac{G_v}{1+G_v\tilde{G}_cK_v}\right)i_{\text{load},q}, \tag{13}$$

where $S(s)$ and $T(s)$ denote the sensitivity and complementary sensitivity transfer functions, respectively and $S(s)+T(s)=1$. Moreover, the DC-gains of these transfer functions for the aforementioned choice of inner-outer controllers are obtained as:

$$|T(j0)| = 1, \ |S(j0)| = 0, \text{ and } |(G_vS)(j0)| = 0.$$

Note that the disturbance signal (load current) appears in (13) through G_vS. And since $|G_vS|$ is small at low-frequencies, the effect of disturbance on output voltage is negligible in the proposed control design, and therefore $V_d \approx V_{\text{ref},d}$ and $V_q \approx V_{\text{ref},q}$ at low frequencies. In fact in the $d-q$ frame, the

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quantities $V_{\text{ref},d} = \hat{V}$ and $V_{\text{ref},q} = 0$ (i.e., the reference signals are DC). Therefore, the proposed controller achieves precise voltage regulation in presence constant (but unknown) output loads. In the next section, we extend the proposed design to a network of parallel inverters with emphasis on active and reactive power sharing.

IV. EXTENSION TO PARALLEL INVERTERS

A microgrid facilitates integration of multiple DERs through a network of parallel inverters to enable higher power output. Economic considerations often dictate that power provided by the sources should be in a certain proportion or according to a prescribed priority. In this section, we describe a droopless control framework for voltage (and frequency) regulation and power sharing that build upon our prior work on control of a network of DC-DC converters [1]. We assume *isochronous* mode of operation of parallel inverters, i.e., a common time reference is assumed for all inverters. Isochronous operation ensures that each inverter has access to the same time-domain voltage reference signal V_{ref}. In practice, isochrony is ensured through sequential synchronization of inverters using phase locked loops (PLLs). In our evaluations in the next section, we employ second-order generalized integrator PLL (SOGI PLL) for synchronization and generating orthogonal components [16].

Consider a network of N parallel connected inverters. Let $\gamma_P^{(1)} : \gamma_P^{(2)} : \cdots : \gamma_P^{(N)}$ and $\gamma_Q^{(1)} : \gamma_Q^{(2)} : \cdots : \gamma_Q^{(N)}$ denote the specified ratios in which DERs are required to apportion their output powers. Here $\gamma_P^{(k)}, \gamma_Q^{(k)} \geq 0$ and $\sum_k \gamma_P^{(k)} = \sum_k \gamma_Q^{(k)} = 1$. Fig. 4 shows the proposed droopless control framework for a system of N parallel inverters connected at the PCC through an output capacitor C. Note that for arbitrary choices of inner and outer controllers, $\{K_{c_k}^{(P)}, K_{v_k}^{(P)}\}$ (for d component) and $\{K_{c_k}^{(Q)}, K_{v_k}^{(Q)}\}$ (for q component), dynamics of a network of parallel inverters becomes highly coupled and intractable. Thus, we impose a *structured* control design, where we set inner controllers $K_{c_k}^{(P)} = K_{c_k}^{(Q)} = K_{c_k}$, as given in (7), for all $k \in \{1, \ldots, N\}$. On the other hand, outer controllers are chosen as $K_{v_k}^{(P)} = \gamma_P^{(k)} K_v$ and $K_{v_k}^{(Q)} = \gamma_Q^{(k)} K_v$ for all $k \in \{1, \ldots, N\}$ to reflect the sharing objective, where K_v is given in (9). The specific choice of inner and outer controllers renders the coupled multi-inverter system in Fig. 4 to an *equivalent* single inverter system shown in Fig. 3, thereby making the stability and performance analysis tractable by reducing the network to a single inverter system. This statement is made precise in the following theorem:

Theorem 1: Consider a single inverter system shown in Fig. 3b with parameters L and R, capacitance C, and compensators K_c and K_v as described in (7) and (9), respectively; and a network of parallel inverters shown in Fig. 4 with same capacitance C, but distinct inverter system parameters $\{L_k, R_k\}_{k=1}^N$, inner controllers $K_{c_k} = \tau^{-1}(L_k + R_k/s)$ and outer controllers $K_{v_k}^{(P)} = \gamma_P^{(k)} K_v$, $K_{v_k}^{(Q)} = \gamma_Q^{(k)} K_v$, where K_v is same as described in (9), such that $\sum_{k=1}^N \gamma_P^{(k)} = \sum_{k=1}^N \gamma_Q^{(k)} = 1$.

1. [Performance equivalence]: Compensators K_{v_k} and K_{c_k} yield *identical* (to single inverter system) performance for a network of multiple parallel inverters connected at the PCC. More precisely, for given exogenous inputs $V_{\text{ref},d}, V_{\text{ref},q}, i_{\text{load},d}, i_{\text{load},q}$, the steady state regulated signals $(V_{\text{ref},d} - V_d, V_{\text{ref},q} - V_q, i_d, i_q, V_d, V_q)$ are identical to the regulated signals $(V_{\text{ref},d} - V_d, V_{\text{ref},q} - V_q, \sum_{k=1}^N i_{d_k}, \sum_{k=1}^N i_{q_k}, V_d, V_q)$ for the system of parallel inverters.

2. [Power Sharing]: The steady-state output active and reactive powers at the PCC get apportioned in the ratios $\gamma_P^{(1)} : \gamma_P^{(2)} : \cdots : \gamma_P^{(N)}$ and $\gamma_Q^{(1)} : \gamma_Q^{(2)} : \cdots : \gamma_Q^{(N)}$, respectively. Thus in the absence of any measurement noises or parametric uncertainties, the proposed design achieves precise voltage (and frequency) regulation and power sharing.

Proof: See appendix.

V. CASE STUDIES: SIMULATIONS AND DISCUSSIONS

In this section, we evaluate the proposed decentralized control scheme for a range of simulated scenarios. These simulations are carried out using Matlab/Simulink and SimPower/SimElectronics library. These simulations are made challenging by incorporating non-ideal components (such as inductors, capacitors) and parametric uncertainties in our models. It should be noted that experiments are underway, hence experimental results are not reported in this paper.

For simulations, we consider a network of three inverters, paralleled together at the PCC. Each inverter is interfaced with the corresponding DC-link, which is regulated at approximately 250V. Robustness of the proposed control design is well tested through demanding scenarios, which include large uncertainties in inductances and capacitance ($\sim 20\%$), (unknown) fast time-varying loads and sensor measurement noise. Below we give a brief overview of parameters used in our evaluations.

Inverter Parameters:

- Input-voltage: $(V_{dc_1}, V_{dc_2}, V_{dc_3}) = (260, 250, 240)$ V
- Inductance: $(L_1, L_2, L_3) = (1.2, 0.8, 1.1)$mH
- Resistance: $(R_1, R_2, R_3) = (1, 0.8, 1.2)m\Omega$
- AC-link Capacitance: $C = 1.2\mu$F

In order to illustrate the robustness of controllers to parametric uncertainties, values of inductance and capacitance for controller synthesis are chosen as $L = 1$mH, $C = 1\mu$F and $R = 1m\Omega$, which are different from their true values. The design parameter for inner loop is chosen by $\tau = 0.2$ms, which results in inner-loop PI controller $K_c(s) = \dfrac{5(s+1)}{s}$. The choice for outer-loop controllers is described in (9) and is given as: $K_v = \dfrac{0.0017(s + 561.5)}{s}$.

Results: By incorporating the methodology described in the previous section, the controllers derived for single inverter system are extended to a network of parallel inverters. Moreover, we also include noise (high-frequency as well as DC offset) in voltage and current sensor measurements

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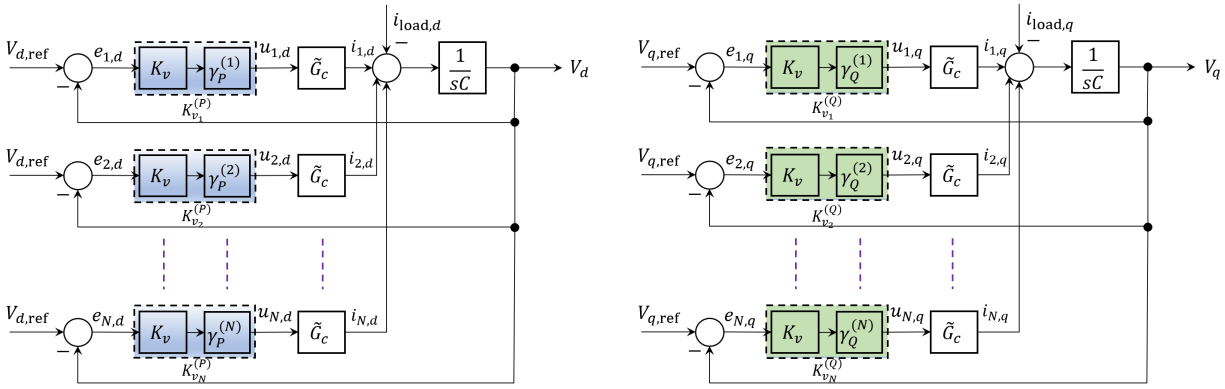

Fig. 4: Proposed control design for a network of parallel inverters for voltage regulation and active-reactive power sharing. The inner controllers K_{c_k} are chosen such that the inner shaped plants for both $d-q$ loops are identical. The outer controllers are scalar multiples of nominal outer loop compensator K_v to reflect (a) active power sharing, and (b) reactive power sharing. The scalars $\{\gamma_P^{(k)}\}$, $\{\gamma_Q^{(k)}\}$ dictate the power-sharing requirements in a network of parallel inverters.

to indicate the ability of controllers of being insensitive to measurement noise. In order to demonstrate effectiveness of the proposed control architecture in maintaining active and reactive power sharing in specified ratios while simultaneously regulating the PCC voltage under uncertain load and measurement noise, we consider two test scenarios:

Test Case 1:

- (Active, Reactive) : (240 W, 240 var)
- Active Power Sharing Requirements:
  1) $(0.33 : 0.33 : 0.33)$, $\quad t < 10s$
  2) $(0.5 : 0.25 : 0.25)$, $\quad 10s \leq t \leq 30s$
- Reactive Power Sharing Requirements:
  1) $(0.33 : 0.33 : 0.33)$, $\quad t < 20s$
  2) $(0.25 : 0.25 : 0.5)$, $\quad 20s \leq t \leq 30s$
- Desired Output Voltage: $V_{\text{ref}} = 120V$ RMS

Test Case 2:

- Active Power Conditions:
  1) 240 W, $\quad t < 10s$
  2) 180 W, $\quad 10 \leq t \leq 30s$
- Reactive Power Conditions:
  1) 240 var, $\quad t < 20s$
  2) 120 var, $\quad 20 \leq t \leq 30s$
- Active & Reactive Power Sharing Requirements: $(0.33 : 0.33 : 0.33)$
- Desired Output Voltage: $V_{\text{ref}} = 120$ RMS

A. Test Case 1: Equal and heterogeneous power sharing

This test case evaluates the ability of controllers in maintaining active and reactive power sharing *independently* according to predefined sharing ratios while regulating PCC voltage for a network of three parallel inverters. In particular, we consider two different sharing requirements on both active as well as reactive power, as indicated in the test-case parameters table. While the proposed control scheme is designed to work seemingly well for a fixed power sharing specification, we in fact impose the dynamic power sharing requirements by updating the sharing ratios to the modified values during the course of simulation. The analysis of transient stability for dynamical power sharing is part of our future work, however, our simulations suggest that the overall network has stable transient behavior. Initially all inverters are required to provide equal active and reactive powers at their output. At $t = 9.9$s, the sharing requirements are changed from $[1 : 1 : 1]$ (equal) to $[2 : 1 : 1]$ (heterogeneous). As shown in Fig. 5a, the proposed control scheme seamlessly adapts to change in sharing requirements through appropriate modification of $\{\gamma_P\}$. Meanwhile, the it is still desired that the inverters share their reactive power equally. This is seen in Fig. 5b that inverters continue to provide equal reactive power. At $t = 19.9$s, the requirements in reactive power sharing are altered to $[1 : 1 : 2]$, while keeping the active power sharing requirements to its current value. Through suitable modification of $\{\gamma_Q\}$, the control design exhibits desired reactive power sharing performance, independent of the active power sharing requirement, as shown in Figs. 5a and 5b. The associated voltage and current waveforms in the $\alpha - \beta$ (fixed) frame are indicated in Figs. 5c and 5d. It is worth noting that the AC-voltage is regulated at 120V rms throughout the simulation. Thus, the proposed control scheme exhibits precise *dynamic* active and reactive power sharing capability, while ensuring voltage regulation in presence of uncertain load.

B. Test Case 2: Time-varying load

In this test case, we evaluate the effectiveness of controllers in ensuring precise power sharing and regulation of voltage at the PCC under uncertain, *time-varying* load. While the converters are desired to share their active and reactive powers equally, load at the PCC is varied through step-changes from $[240\text{W}, 240\text{var}]$ to $[180\text{W}, 240\text{var}]$ at $t = 10$s

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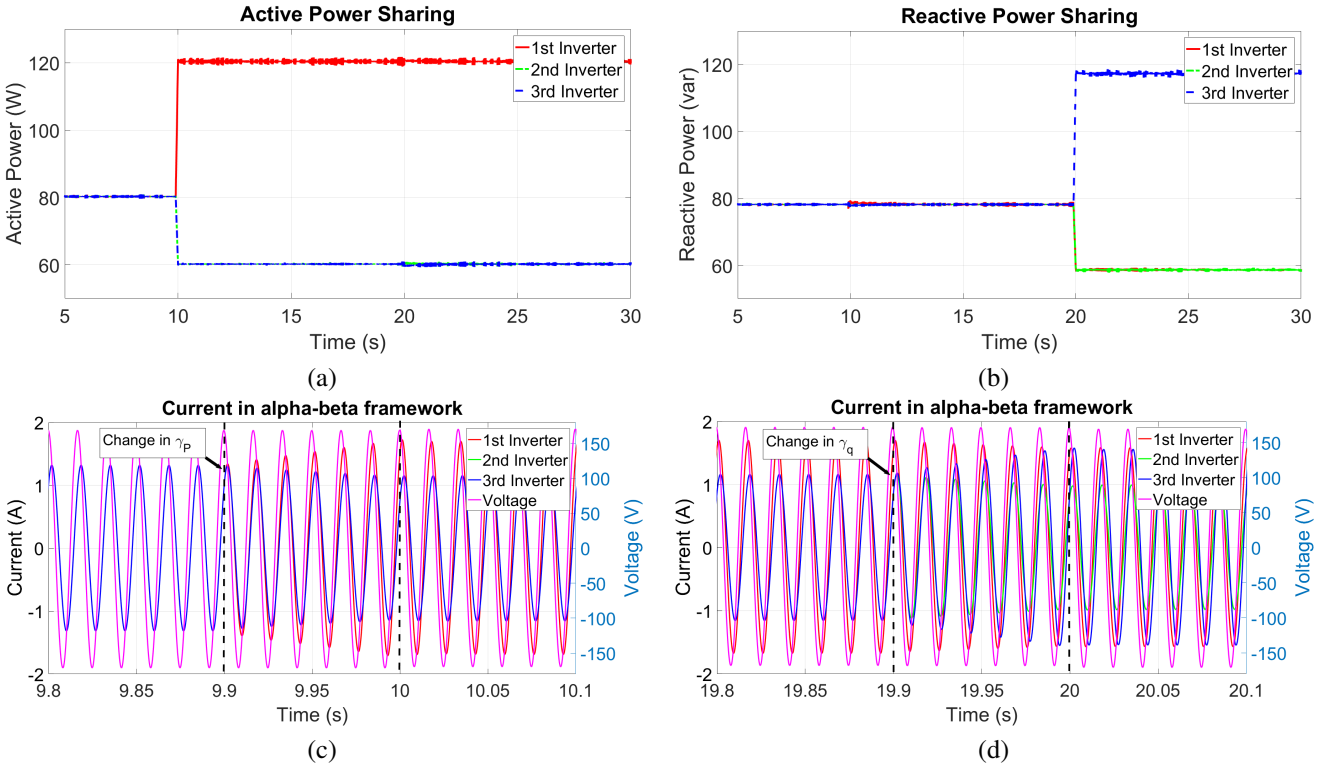

Fig. 5: (a) Active and (b) Reactive power outputs of the inverters. Output voltage and current waveforms during change in (c) active and (d) reactive power sharing requirement. The proposed control scheme exhibits precise *dynamic* active and reactive power sharing capability, while ensuring voltage regulation in presence of uncertain load.

and then to $[180\text{W}, 120\text{var}]$ at $t = 20$s. As shown in Figs. 6a and 6b, the inverters continue to share their active and reactive powers equally even when the loading conditions are abruptly altered. Figs. 6c and 6d depict the output voltage and current waveforms in the fixed frame. As with the previous test case, the output voltage is maintained at 120V rms. Thus the capability of the proposed control design in ensuring precise regulation and power sharing in presence of uncertain and time-varying loads is validated.

VI. CONCLUSIONS AND FUTURE WORK

In this paper, a novel, droopless, decentralized and scalable control architecture for a network of parallel inverters for precise voltage regulation, and active and reactive power sharing. The proposed methodology overcomes limitations of droop-based control schemes both in terms of dynamic response to tracking and power sharing. Moreover, the stability and performance of network is analyzable in terms of an equivalent single-inverter system, thereby considerably reducing the complexity of coupled multi-inverter system. Decoupling feed-forward terms are used to separate out the sharing objectives on active and reactive powers. The hardware setup to demonstrate the proposed control architecture is under preparation and the experimental results will soon be reported in our subsequent work.

APPENDIX

Theorem 1 is derived only in the context of d-axis control loop. Results for q-axis control loop follow similarly.

Proof of Theorem 1: System Equivalence

Proof: Let $\tilde{G}_c$ denote the inner shaped plant for the single inverter system. For the single inverter system, the voltage at the PCC is described in (13). Therefore the tracking error $e_d \triangleq V_{\text{ref},d} - V_d$ is given by:

$$V_{\text{ref},d} - V_d = SV_{\text{ref},d} + G_v S i_{\text{load},d}. \tag{14}$$

On the other hand, for the network of parallel inverters shown in Fig. 4a, the d component of the AC-side voltage is given by:

$$V_d = G_v \left(\sum_{k=1}^{N} \gamma_P^{(k)} \tilde{G}_c K_v (V_{\text{ref},d} - V_d) - i_{\text{load},d} \right). \tag{15}$$

Using the fact that $\sum_{k=1}^{N} \gamma_P^{(k)} = 1$, and from (15) one obtains:

$$V_d = TV_{\text{ref},d} - G_v S i_{\text{load},d}, \tag{16}$$

where T and S are defined in (13). (16) is identical to (13) and thus yields identical expression for tracking error $V_{\text{ref},d} - V_d$ as well. Similarly, the d component of inverter current i_d in the single inverter case in Fig. 3b is given by:

$$i_d = \tilde{G}_c K_v (V_{\text{ref},d} - V_d). \tag{17}$$

On the other hand, the inverter current i_{d_k} for the k^{th} inverter in Fig. 4a is given by $i_{d_k} = \gamma_P^{(k)} K_v (V_{\text{ref},d} - V_d)$. Summing it over k yields $\sum_{k=1}^{N} i_{d_k} = \tilde{G}_c K_v (V_{\text{ref},d} - V_d) = i_d$, which establishes the required equivalence. ■

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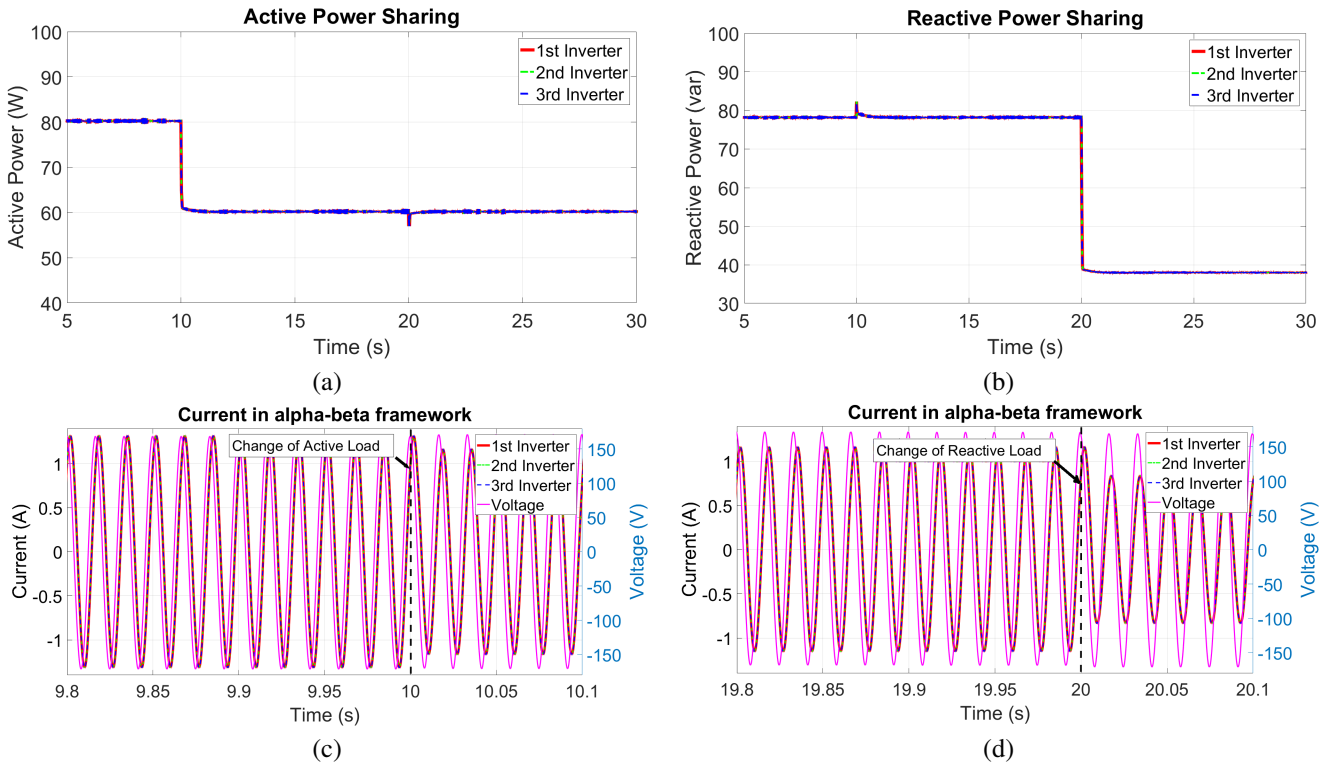

Fig. 6: (a) Equal sharing is maintained during sudden change in (a) active and (b) reactive loads. Output voltage and current waveforms during changes in (c) active and (d) reactive loads. The proposed control scheme exhibits precise active and reactive power sharing capability, while ensuring voltage regulation in presence of uncertain and time-varying load.

Proof of Theorem 1: Power Sharing

Proof: The power sharing scheme follows directly from the construction. Note that the d-component of the inverter current is given by $i_{d_k} = \gamma_P^{(k)} K_v (V_{\text{ref},d} - V_d)$. Thus, for inverters j and k, we have $\dfrac{i_{d_j}}{\gamma_P^{(j)}} = \dfrac{i_{d_k}}{\gamma_P^{(k)}}$. On the other hand, from (4), the real power is related only to the d-component of the current, and thus the inverters apportion their active powers in the ratio $\gamma_P^{(1)} : \gamma_P^{(2)} : \cdots : \gamma_P^{(N)}$. A similar conclusion holds for reactive power sharing, too, albeit in the ratio $\gamma_Q^{(1)} : \gamma_Q^{(2)} : \cdots : \gamma_Q^{(N)}$. ■

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